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Stability Analysis of Limit Cycles in High Order Sigma Delta Modulators

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ABSTRACT

We present a mathematical framework, based on state space modelling, for the description of limit cycles of Sigma Delta Modulators (SDMs). Using a dynamical systems approach, the authors treat sigma delta modulators as piecewise linear maps. This enables us to find all possible limit cycles that might exist in an arbitrary sigma delta modulator with predefined input. We then focus on a DC input analyse their stability and show exactly the amount of dither that is necessary to remove any given limit cycle. Using several different SDM designs, we locate and analyse the limit cycles and thus verify the results by simulation.

1. INTRODUCTION

Although many aspects of sigma delta modulation can be understood in the approximation of linear modelling the device(see, for example, [1]), limit cycles (LCs) are a phenomenon occurring in sigma delta modulators (SDMs) which can not be explained in this model. There have been several important advances towards a theory of limit cycles[2-4], but there is no unified description[5]. Instead, different models are applicable to different SDM designs, with limited results.

In practical implementations it is important that measures are known to sufficiently prevent limit cycles. In order to be able to achieve this, proper understanding of the phenomenon is mandatory. The work described in this paper aims at exactly this, thus handing the practical engineer the necessary tools to design and build a modulator, without the need to perform numerous simulations afterwards to check for phenomena such as limit cycles.

2. LIMIT CYCLES

2.1. State Space Description

A highly convenient way to describe the time domain behaviour of an SDM is the state space description. This represents the state of the SDM at any time as a matrix operation applied to the state at the previous clock cycle. The power of the state space description

is that it allows us to create a very compact description of the propagation of the SDM from time t=0 to time t=n.

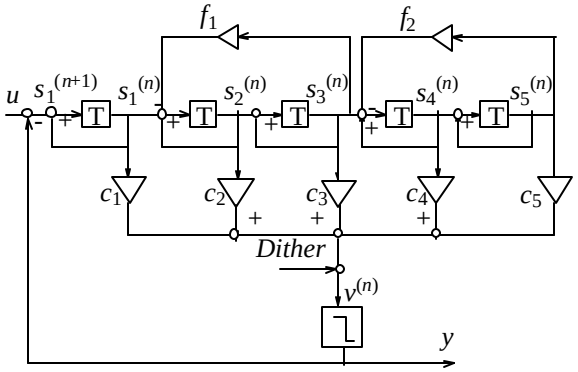

Figure 1. States in a 5th order SDM.

For an N^{th} order SDM,

$$s^{(n+1)} = \mathbf{A}\, s^{(n)} + (u^{(n)} - y^{(n)})\, \mathbf{d} \qquad (1)$$

where (ignoring dither)

$$v^{(n)} = \sum_{i=1}^{N} c_i s_i^{(n)} = \mathbf{c}^T \mathbf{s}^{(n)}$$
$$y^{(n)} = \mathrm{sgn}(v^{(n)}) \qquad (2)$$

A is the transition matrix and **d** describes how input and feedback are distributed. This description gives the state of the SDM in terms of a transition matrix applied to the previous state vector, and a vector applied to the scalar quantisation error, $u^{(n)}$-$y^{(n)}$.

For the 5th order modulator described in Figure 1, $\mathbf{d}=(1,0,0,0,0)^T$ and the transition matrix is

$$\mathbf{A} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -f_1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & -f_2 \\ 0 & 0 & 0 & 1 & 1 \end{pmatrix} \qquad (3)$$

Repeated application of (1) leads to

$$s^{(n)} = \mathbf{A}^n\, s^{(0)} + [\sum_{i=0}^{n-1} (u^{(i)} - y^{(i)})\mathbf{A}^{n-i-1}]\, \mathbf{d} \qquad (4)$$

From this representation, we see that the initial integrator states are an offset to the signal. The spectrum of the signal is determined completely by terms independent of the initial state. Hence, this confirms the known fact that the signal content of a modulator is not determined by its initial integrator states.

2.2. Limit Cycle Conditions

The compact representation gives the means to directly view the consequences of a limit cycle. If the limit cycle has period P we have, by definition,

$$\mathbf{s}^{(n+P)} = \mathbf{s}^{(n)} \qquad (5)$$

By combining, (5) and (4), and rearranging terms, we obtain

$$s^{(n)} = (\mathbf{I} - \mathbf{A}^P)^{-1}[\sum_{i=0}^{P-1} (u^{(i)} - y^{(i)})\mathbf{A}^{n-i-1}]\, \mathbf{d} \qquad (6)$$

As a consequence, we have a strict set of necessary (but not sufficient!) equalities that need to hold for the initial states if such a limit cycle is sustained.

From this, we can obtain a unique value for the initial state $s^{(0)}$ if, and only if, the inverse of the matrix ($\mathbf{I} - \mathbf{A}^P$) exists. We assume that a solution or solution space exists.

So far, the appearance of the limit cycle has not been specified, except that it is of period P. However, if the limit cycle is now defined as a sequence of quantiser inputs, we can produce a set of inequalities required by the limit cycle. For each y_i,

$$v_i y_i = \mathbf{c}^T \mathbf{s}^{(i)} > 0 \qquad (7)$$

For SDMs which do have a pole at DC, and thus have infinite gain for DC, the sequence also completely determines the input $u = u(i)$ to the SDM in case the input is a DC value.

$$u^{(i)} \equiv u = \frac{1}{P}\sum_{i=0}^{P-1} y^{(i)} \qquad (8)$$

The inaccuracy made here is that the possibility that $v(i)y(i) = 0$ has been left out. As this equality occurs with probability zero over the continuously variable value of $v(i)y(i)$, this is supposed to be not much of a problem. We thus have a set of equalities, and a set of inequalities that need to be fulfilled in order to have a valid limit cycle.

3. Disturbing the limit cycle

In the previous section, the remark has been made that the matrix ($\mathbf{I} - \mathbf{A}^P$) may not be invertible. This is a rather interesting observation, which can be exemplified by the following. The zeroes of the NTF of a SDM are given by the eigenvalues of the transition matrix **A**. Hence, for a classical SDM which has all its loop filter poles at DC, all eigenvalues of A will be one, as a result of which the inverse does not exist - hence, there is no unique solution to $\mathbf{s}^{(0)}$. On the other hand, if we have a SDM of even order O resonator sections, all loop filter poles will occur for frequencies other than DC. As a result, there will exist one - and one only – initial state $\mathbf{s}^{(0)}$ that results in a limit cycle of period P! Most often, SDMs have at least a single zero at DC to avoid DC drift. In the following, we will make a separation in two main categories of SDMs: those with and without poles at DC. The SDMs with poles at DC will be further subdivided in two categories: those with poles at DC for the last two integrator

sections; and those with poles away from DC for the last two integrator sections.

3.1. SDMs with DC Poles

In the case that the SDM has at least one of its poles at DC, the matrix $(\mathbf{I} - \mathbf{A}^P)$ is singular, and, hence, not invertible. To still solve (6) for that case, we create the singular value decomposition (SVD) of $(\mathbf{I} - \mathbf{A}^P)$[6]:

$$\mathbf{I} - \mathbf{A}^P = \mathbf{U}\Sigma\mathbf{V}^T \qquad (9)$$

The matrices $\mathbf{U}$ and $\mathbf{V}$ are the left and right singular vectors, respectively, and Σ is a diagonal matrix containing the singular values of $(\mathbf{I} - \mathbf{A}^P)$. When the SDM is not reducible, exactly one of the singular values will be zero. This has the interesting consequence that the last column of $\mathbf{V}$, i.e., the null space of $(\mathbf{I} - \mathbf{A}^P)$, is a non-relevant direction since it is always multiplied by zero. Thus the complete set of solutions is a line.

The SVD comes in helpful too, in obtaining an initial solution $\mathbf{s}_{mn}$ as a minimum norm solution. For each inequality we can write an equality which determines a critical distance from the initial point $\mathbf{s}_{mn}$ at which the k^{th} constraint is on the edge of being violated. The distance is a measure for the maximum disturbance that can be applied to a limit cycle before it breaks up.

We will now investigate the nature of the disturbance that can be applied to the SDM, before the limit cycle breaks up. We will separate this for SDMs with only DC poles, and SDMs with at least one DC pole.

3.1.1.Last integrators with DC Poles

The question that needs to be answered is what the null-space looks like. For the current case, we have DC poles for the last two integrator sections, which translates to the fact that the last column of the transition matrix $\mathbf{A}$ is given by $(0, 0, \ldots 0, 1)$. This means that we can alter the state of the last integrator over a range without breaking up the limit cycle. However, the effect of changing the last integrator state is nothing else but adding dither just before the quantizer, as depicted in Figure 1. For example, when the last integrator state is changed by an amount δ, this is equivalent to adding a value $c\delta$ to the input of the quantizer. Thus, the approach in Sec. 2 provides us with the means to define a minimum dither level which is necessary to break up a limit cycle.

3.1.2.At least one DC Poles (but not made by last 2 integrators)

In case the last two integrator sections form a resonator, the null space doesn't have the simple shape anymore as in the previous section. In fact, if the feedback coefficient in the last two integrator sections equals f, it can be shown that to very good approximation the null-space is given by $v0 = (0,\ldots f, 0, 1)^T$ Hence, in order not to disturb a limit cycle when changing the last integrator section, the third integrator state should also be changed. Although it is not as easy to define the exact minimum level of dither that needs to be added to the quantizer (i.e., change the last integrator state), it still is possible to define a value of dither which is at equal or larger than the minimum amount.

3.2. No DC Poles

A special situation arises when the SDM has no DC poles. In that case, the null space is zero: there is only one solution. If this solution also complies with all inequalities, this solution results in a limit cycle. Because the null space is zero, any change of the integrator states would result in a break-up of the limit cycle.

4. EXAMPLES

The results of the work detailed in the preceding part, have been used to obtain some results on 4 different Noise transfer functions (NTFs), which have been implemented in both feedforward as well as feedback SDMs. The SDMs are indicated in the table below.

Table 1. List of SDMs analysed in simulation, and their corresponding codes in the text.

NTF Type	Code
Aggressive, with resonators	1a
Aggressive, without resonators	1b
Non-aggressive, with resonators	2a
Non-aggressive, without resonators	2b

In the following sections, we will discuss results for both SDM types (which implement identical NTFs) to judge whether how the implementation topology influences the limit cycle behaviour.

4.1. Feedforward SDMs

In Figure 2, the occurrence of limit cycles as a function of the feedback coefficients is presented. The figure represents all independent limit cycles1 that could exist with lengths ranging from 3 to 30 bits. All possible DC values are represented by these limit cycles, and it should be mentioned that, while some of these limit cycles theoretically exist, cannot occur in practice. For example, it is possible to define a limit cycle corresponding to an input of 0.9, where none of the SDMs studied would be capable of representing this DC level without running into instability.

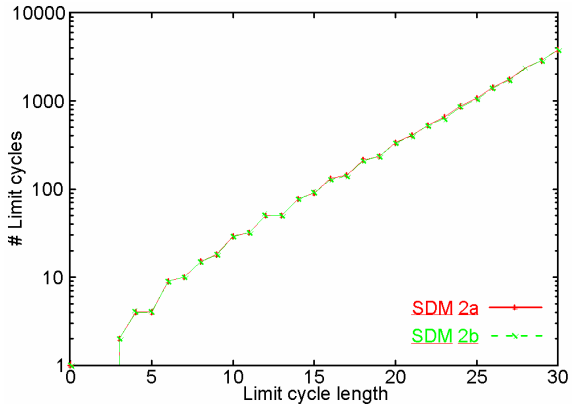

Figure 2 Occurrence of limit cycles of SDM 2a and 2b.

It is apparent immediately from Figure 2, that the presence or absence of resonator coeficients is immaterial to the number of limit cycles that can occur. The same is approximately true when comparing SDM 1a and 1b (not shown). However, this is not so anymore when comparing the aggressive SDM 1a and the non-aggressive SDM 2a in Figure 3.

Rather counterintuitive, the SDM 1a displays more limit cycles than SDM 2a; one would expect the reverse to be true. While the number of limit cycles for SDM 2a is increasing exponentially, SDM 1a shows two different regions, where up to a limit cycle length of about 20, the number of possible limit cycles increases exponentially. For larger limit cycles, the growth reduces significantly - and, in fact, one could wonder whether at some point the two curves in Figure 3 cross.

While the absolute number of limit cycles increases rapidly, relative to the number of possible permutions of +1s and -1s it is reducing rapidly as is demonstrated in Figure 4. The total number N_P of permutations for a limit cycle of length P is approximately given by[3]:

$$N_P \approx 2^P / P \qquad (10)$$

The division by P corrects for the fact that of all 2P permutations, exactly P represent a cyclicly shifted version of the same basic limit cycle. To obtain the exact number of irreducible limit cycles, correction should be made too for the number of limit cycles that are a concatenation of smaller limit cycles. However, for reasonable P, this number is much smaller compared to N_P and thus ignored.

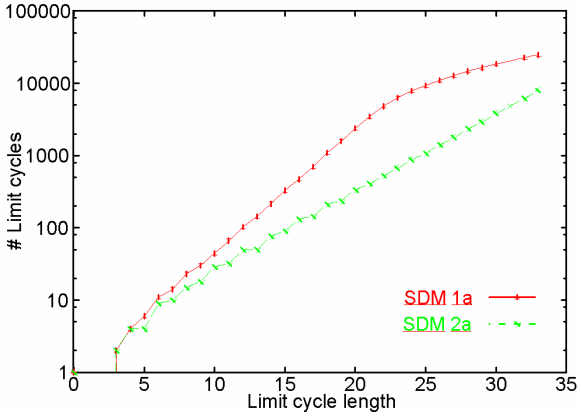

Figure 3 Occurrence of limit cycles of SDM 1a and 2a.

In Figure 5, the minimum dither level that is needed to certainly break up the most stable limit cycle is depicted. In red and blue, the most stable limit cycle for SDM 1a and 2a, respectively, for DC input is depicted. While slightly more stable limit cycles can sometimes be found for non-DC inputs, these situations do not represent a practical situation. The first interesting observation is that the limit cycles for the aggressive SDM 1a are more stable than those of the less aggressive SMD 2a. This is quite counter-intuitive. Also, we can see that there is a very stable limit cycle occurring around limit cycle length 22 for SDM 1a, and for limit cycle length 32 for SDM 2a. Upon investigation of these limit cycles, it appeared that they consist of a series of 11 1s followed by 11 -1s for SDM 1a, and likewise 16 1s and 16 -1s for SDM 2a. This corresponds to a square wave of frequency 120 kHz and 80 kHz, respectively, which are exactly the corner frequencies of the NTF design of the SDMs. In practice, however, these limit cycles could never occur; upon the slightest disturbance of the integrators, the SDM becomes unstable.

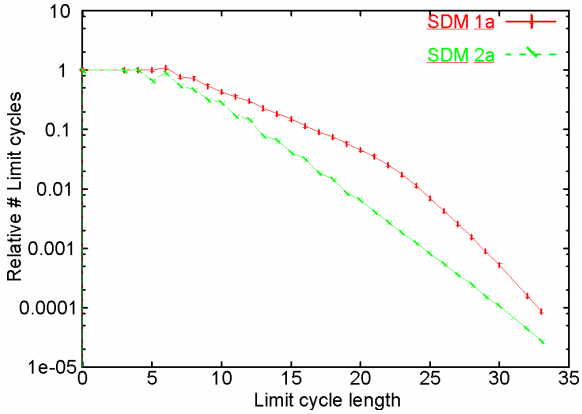

Figure 4 Relative occurrence of limit cycles of SDM 1a and 2a with respect to all permutations of bits.

This is to be contrasted with the limit cycle behavior for other limit cycle lengths. The shortest limit cycle, the sequence {1,-1}, appears to be most stable (disregarding the previously discussed limit cycles) for both SDMs. For longer limit cycles, the amount of dither needed for break-up decreases to a minimum value close to the peak, after which the limit cycle becomes more stable. All these limit cycles consist of the sequence {-1,1,-1,1, ... -1,1,-1,-1,1,1}, which represents the minimally possible deviation for the simple {-1,1} sequence. While these most stable limit cycles slightly increase in stability for longer limit cycles, on average the amount of dither necessary for break-up decreases. This is indicated in green and magenta for SDM 1a and 1b, respectively, in Figure 5. The average amount of dither is defined as the average of the minimum dither levels that are needed to break up the individual limit cycles. Again, we see that SDM 1a presents limit cycles that are in general more stable than those of SDM 2a. At limit cycle lengths of 42, the average amount of dither is reduced to about 0.03 and 0.017 for SDM 1a and 2a, respectively, which is consists with the intuition that longer limit cycles represent more boundary conditions to be fulfilled and are thus more easy to break up.

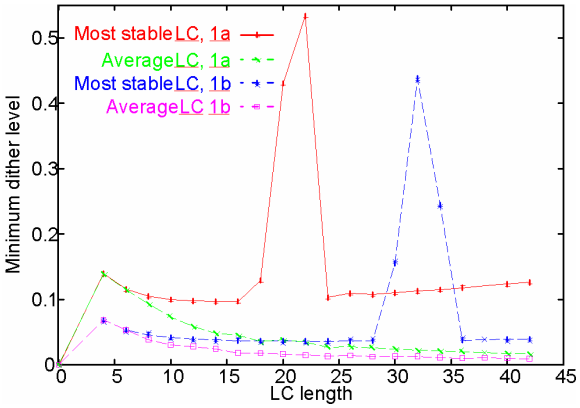

Figure 5. Minimum level of dither needed to break up a limit cycle corresponding to DC input zero.

Another interesting characteristic to study is the relative preference of the SDM for limit cycles of a certain DC level. These results are displayed in Figure 6 through 8 Conforming to the results in Figure 3, in general SDM 1 exhibits many more possible limit cycles for any DC level than SDM 2. Also, we see that (as anticipated) the number of limit cycles is identical for a certain DC level and the negative DC level. However, whereas SDM 1 has strong preference for limit cycle with small absolute DC level, SDM2 apparently has little preference! Moreover, where SDM 2 displays little dependence on the presence of resonator sections, SDM 1 shows, especially for the smallest DC levels some dependence, displaying most limit cycles when no resonators are present. The reason for this behavior is unclear.

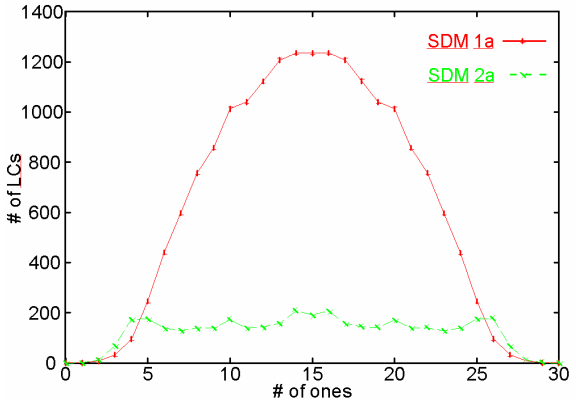

Figure 6. Occurrence of limit cycles as a function of the number of ones in the limit cycle for SDM 1a and 2a.

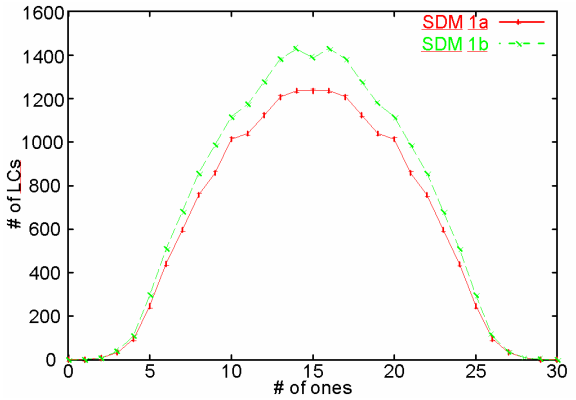

Figure 7. Occurrence of limit cycles as a function of the number of ones in the limit cycle for SDM 1a and 1b

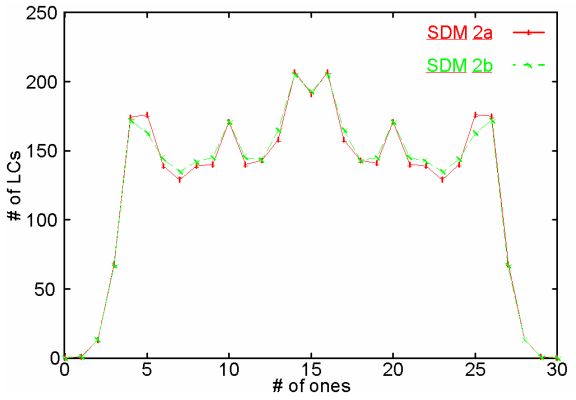

Figure 8. Occurrence of limit cycles as a function of the number of ones in the limit cycle for SDM 1a and 2b.

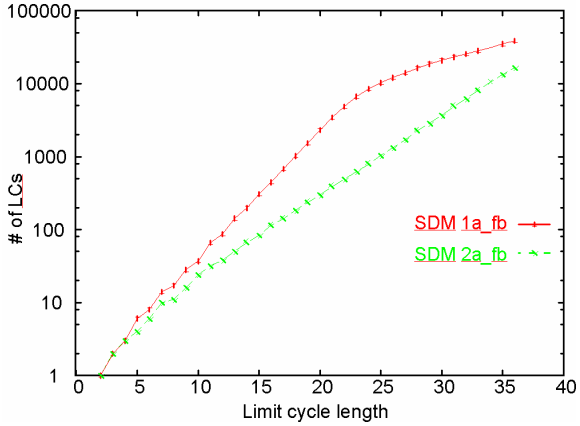

Figure 9. Occurrence of limit cycles for SDM 1a_fb and 2a_fb.

4.2. Feedback SDMs

In order to see how much of the limit cycle behavior is determined by the implementation of the NTF in either a feedforward or feedback structure, we have performed some calculations on SDMs in feedback topology, which implement identical NTFs as those of SDM 1a and 2a[7]. We will refer to these SDMs as 1a_fb and 2a_fb.

In Figure 9, the occurrence (for all DC values) of limit cycles is indicated. When we compare these results to the equivalent for a feedforward SDM, Figure 3, hardly any difference in behaviour can be observed. Perhaps even more informative is the comparison with the stability of limit cycles. The equivalent of Figure 5 for feedback type SDMs also reveals a close correspondence between both topologies.

5. CONCLUSION

This work is an attempt to construct and apply a theory describing limit cycles in sigma delta modulators. It has been shown that limit cycle behavior can occur in a wide variety of situations, often with unexpected results. This paper differs from previous work in that it is not limited to specific modulator designs, strong constraints on the limit cycle, or unproven conjectures. We have been able to quantify how common the existence of limit cycles is for a given design, (in general need at least *n*-1 init conditions filled) how stable they are, and how much dither is required to remove them. Ongoing work concerns how to put these results onto a more rigorous mathematical basis, as will be shown in a forthcoming paper.

6. REFERENCES

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